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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,158	09/26/2001	Martin Li	TI-33430	9577

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EXAMINER	
GREY, CHRISTOPHER P	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/964,158	LI ET AL.	
	Examiner	Art Unit	
	Christopher P. Grey	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 5 is objected to because of the following informalities: Line 2 of claim 5 recites, " can be" which is not a positive recitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 7, 8, 10 rejected under 35 U.S.C. 102(e) under 35 U.S.C. 103(a) as obvious over Jensen et al. (US 6732206) in view of Chen et al. (US 5870628), hereinafter referred to as Chen.

Claim 1 Jensen et al. ('Jensen' hereinafter) discloses an ATM cell being transmitted from a Master unit (element 10 in fig1). Jensen discloses a slave unit (element 14 in fig 1) receiving the ATM cell (Col 2 lines 8-24). Jensen also discloses a bus for exchanging information between master and slave units (element 12 in fig 1).

Jensen discloses a FIFO buffer (element 22 in fig 1) for storing incoming cells where the cells have an encoded destination (Col 2 lines25-34 and Col 2 lines 14-16, internal address and bits equivalent to encoded data).

Jensen discloses an address translation (calculation) unit (element 20 in fig 1) in the ATM slave unit (see fig 1, 14, 20).

Jensen discloses the translation unit including an ATM content addressable memory and look up table (register) as disclosed in Col 2 lines 36-45. Jensen discloses the translation unit accessing this memory and lookup table in order to generate the destination address within the slave (Col 2 lines 8-34).

Jensen does not specifically disclose transferring data from a buffer to a direct memory access unit.

Chen discloses transferring data from a FIFO to a DMA unit see fig 2 and Col 5 lines 1-30).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the DMA controller, channels registers and FIFO's as disclosed by Chen, within the Slave unit as disclosed by Jensen. The motivation for this combination is an alternative way of transferring data from the FIFO (Col 5 lines 32-43).

Claim 2 Jensen discloses a FIFO buffer (element 22 in fig 1) for storing incoming cells (Col 2 lines25-34).

Claim 3, 16 Jensen discloses a FIFO unit capable of holding two cells (Col 2 lines 25-34).

Claim 7 Jensen discloses a slave unit containing a processor (element 18 in fig 1).

Claim 8 Jensen discloses data being passed to a UTOPIA bus (Col 5 lines 28-35).

Claim 10 Jensen discloses a FIFO buffer (element 22 in fig 1) for storing cells incoming from a master unit (Col 2 lines25-34 and see fig 1 elements 10 and 22).

Jensen discloses the translation unit including an ATM content addressable memory and look up table (register) as disclosed in Col 2 lines 36-45.

Jensen discloses the translation unit accessing this memory and lookup table in order to generate the destination address within the slave (Col 2 lines 8-34).

Jensen discloses after address translation, routing the data from the FIFO to their respective destinations (Col 2 lines 25-35).

However, Jensen does not specifically disclose transmitting when storage space is available, a data cell from the buffer storage unit to the direct memory access unit (obvious).

Chen discloses transferring data from the input buffer to a DMA FIFO when the DMA FIFO is available (Col 5 lines 1-31, threshold to ensure availability).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the slave processor as disclosed by Jensen, to inquire about a state of availability as disclosed by Kessler. The motivation for this combination is to avoid failure of delivery due to congestion and delay (Col 6 lines 9-19).

3. Claims 14 and 16 rejected under 35 U.S.C. 102(e) under 35 U.S.C. 103(a) as obvious over Jensen et al. (US 6732206) in view of Schneider et al. (US 7002979), hereinafter referred to as Schneider

Claim 14 Jensen discloses a master processing unit (fig 1 element10).

Jensen discloses a slave processing unit (Fig 1 element 14)

Jensen discloses a bus interfacing a master and slave, where the bus exchanges data between a master and slave (element 12 in fig 1).

The bus is connected to the slave, which consists of a FIFO buffer (element 22 in fig 1) for storing data (Col 2 lines25-34).

Jensen also discloses a an ATM content addressable memory as disclosed in Col 2 lines 36-45

Jensen discloses an address translation (calculation) unit (element 20 in fig 1).

Jensen discloses the address translation unit containing a memory, and the address translation unit connected to the FIFO buffer (Col 2 lines 36-45 and see fig 1)

Jensen discloses a look up table (register) within the address translation unit (Col 2 lines 36-45), where the address translation unit seeks a destination address, and routes data to the address port (Col 2 lines 25-35).

Jensen does not specifically disclose the ATM slave processing device including a DMA and transferring data and control signals from a buffer to a direct memory access unit.

Schneider discloses a slave system (fig 1) including a DMA unit (fig 1, 106) and a receive buffer (fig 10 1006 and fig 1, 112), where the DMA and buffer unit exchange data including control data (Col 6 lines 5-9, arbitrate).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the DMA as disclosed by Schneider to the slave unit, specifically attaching it to the receive FIFO as disclosed by Jensen. The obvious motivation for this

combination is to eliminate heavy overload, as is well known in the art when DMA's are employed.

Claim 16 Jensen discloses a FIFO unit capable of holding two cells (Col 2 lines 25-34).

4. Claims 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Chen et al. (US 5870628), in view of Thomas et al. (US 5941952)

Claim 4 Jensen discloses a clock domain (Col 2 lines 46-65). However Jensen does not disclose the buffer storage unit transferring a data cell to the slave data processing unit every clock cycle.

Thomas et al ('Thomas' hereinafter) discloses circuitry for transmitting data from a buffer unit to an interface at a particular rate (Col2 lines 36-54).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify that master unit as disclosed by Jensen, to include Thomas' circuitry for controlling the data transfer rate to an interface, where the rate may be manipulated based on a user preference, so as to fulfill transferring of data every clock cycle. The motivation for the modification is to transfer data in a timely manner so as to prevent delays (Col 1 lines7-11 and Col 2 lines 6-35).

5. Claims 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Schneider et al. (US 7002979) in view of Thomas et al. (US 5941952)

Claim 17 Jensen discloses a clock domain (Col 2 lines 46-65). However Jensen does not disclose the buffer storage unit transferring a data cell to the slave data processing unit every clock cycle.

Thomas et al ('Thomas' hereinafter) discloses circuitry for transmitting data from a buffer unit to an interface at a particular rate (Col2 lines 36-54).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify that master unit as disclosed by Jensen, to include Thomas' circuitry for controlling the data transfer rate to an interface, where the rate may be manipulated based on a user preference, so as to fulfill transferring of data every clock cycle. The motivation for the modification is to transfer data in a timely manner so as to prevent delays (Col 1 lines7-11 and Col 2 lines 6-35).

6. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Chen et al. (US 5870628), in view of Kessler et al. (6029212).

Claim 5 Jensen discloses using an address translation unit to determine a destination (Col 2 lines 8-24).

However, Jensen does not disclose the destination locations being selected from a group of a plurality of central processing units and memory locations, at least one central processing unit and at least one memory location.

Kessler et al. ('Kessler' hereinafter) discloses a translation unit for calculating an address of a memory location, and transferring the data to one (selected) of a multiple number of external registers (Col 2 lines 5-17), where an external register may be equivalent to and comparable to any of a plurality of processing units, a shared memory location or a combination of both..

It would have been obvious to one of the ordinary skill in the art at the time of the invention to specify the result of the translation (destination) as disclosed by Jensen, to include external registers, where registers are memory oriented and have several processing functions. The motivation for this specification is to address data to a specific location (Col1 lines12-15).

Claim 13 Jensen does not disclose the processing unit including a direct memory access unit, and applying the signal identifying the destination location to the direct memory access unit.

Kessler discloses the slave unit coupled to a direct memory access unit that transmits requests and is coupled to a slave unit (Col 20 lines 40-52).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the slave unit as disclosed by Jensen to include a direct memory access unit as disclosed by Kessler, where a request may be dedicated for retrieving a

destination address. The motivation for this combination is to allow easier and direct access to memory.

7. Claims 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Chen et al. (US 5870628), in view of Schneider et al. (US 7002979), hereinafter referred to as Schneider

Claim 6 The combined teachings of Jensen and Chen disclose a buffer including a storage unit for storing data cells and a master unit in communication with a slave unit as disclosed within the rejection of claim 1.

The combined teachings of Jensen and Chen do not specifically disclose receiving data cells from the direct memory access unit the data buffer unit exchanging control signals with the slave processing direct memory access unit, and an output unit receiving data cells from the output buffer.

Schneider discloses an interface unit (fig 1 elements 102, 104, 108 and 110 make up an interface unit) comprising an output buffer unit **(the network interface 102 has a buffer 1006 in fig 12 for receiving data coming from the DMA 106 in fig 1)** receiving data from the direct memory access unit **(fig 1, 106).**

Schneider discloses the data buffer unit exchanging control signals with the slave processing direct memory access unit **(Col 6 lines 5-8, arbitrate and Col 5 lines 33-35, control info).**

Schneider discloses an output unit receiving data cells from the output buffer **(fig 10 depicts the interface unit shown in fig 1, where the mac core is equivalent to**

an output unit and it receives data from the FIFO and transmits it to another device connected through the MII depicted).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Jensen and Chen with the output buffer and unit for transmitting stored data from a slave unit. The motivation for this modification is to reduce latency between a source and destination **(Col 3 lines 11-12).**

8. Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen et al. (US 6732206) in view of Chen et al. (US 5870628) in further view of Thomas et al. (US 5941952) .

Claim 11 Jensen discloses a FIFO unit capable of holding two cells (Col 2 lines 25-34).

The combined teachings of Jensen and Chen do not specifically transferring a data cell from the buffer storage unit to the ATM slave processing unit on consecutive cycles

Thomas et al ('Thomas' hereinafter) discloses circuitry for transmitting data from a buffer unit to an interface at a particular rate (Col2 lines 36-54).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Jensen and Chen, to include Thomas' circuitry for controlling the data transfer rate to an interface, where the rate may be manipulated based on a user preference, so as to fulfill transferring of data every clock

cycle. The motivation for the modification is to transfer data in a timely manner so as to prevent delays (Col 1 lines7-11 and Col 2 lines 6-35).

Claim 12 Jensen discloses data being passed to a UTOPIA bus (Col 5 lines 28-35).

Response to Arguments

9. Applicant's arguments filed February 16, 2007 have been fully considered but they are not persuasive.

(a) The applicant argued with regards to claims 1, 10 and 14, that the cited art does not disclose the applicant's interaction of an ATM slave processor unit with an ATM master processor unit using the UTOPIA signal format.

The examiner maintains that Jensen discloses a master unit in communication with slave units (fig 1, 10 and 14's). In response to applicants arguments that the references fail to show certain features of the applicants invention, it is noted that the features upon which applicant relies (ie utopia signal format) are not recited in the rejected claims. Although the claims are not interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed Cir. 1993).

(b) The applicant argued with regards to claims 1, 10 and 14 that the cited art does not disclose an interface unit that includes both an input section and an output section (as disclosed in the remarks in lines 28-30).

In response to applicants arguments that the references fail to show certain features of the applicants invention, it is noted that the features upon which applicant relies (ie output section) are not recited in the rejected claims. Although the claims are not interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed Cir. 1993).

The examiner maintains that an input section is disclosed within Jensen (Col 2 lines 13-15, an incoming cell is routed to the address...)

(c) The applicant argued with regards to claims 1, 10 and 14 that the cited art does not disclose the applicants claimed limitation of a two stage FIFO in the input section and in the output section (as disclosed in the remarks on page 9 lines 2-4)

In response to applicants arguments that the references fail to show certain features of the applicants invention, it is noted that the features upon which applicant relies (ie **a two stage** FIFO in the input section and in the **output section**) are not recited in the rejected claims. Although the claims are not interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed Cir. 1993).

The examiner makes note that Jensen discloses a FIFO being used within the slave device.

(d) The applicant argued that it is unclear how Jensen and Chen can be combined.

The examiner maintains that there is clear motivation for the combinations of references, wherein it would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the DMA buffers and controller as disclosed in the network adapter as disclosed by Chen to the slave unit as disclosed by Jensen. To be specific, the DMA buffers better handle dynamic random quantities of data, making the device less susceptible to dropping of packets and errors. The DMA buffers can be combined so as to take the place of the queues (fig 1, 26 and fig 2, 26)

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P. Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571)272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher Grey
Examiner
Art Unit 2616

3/22/07

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